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EXAMINER	
YU, HENRY W	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,132	BOGIN ET AL.	
	Examiner	Art Unit	
	HENRY YU	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/723,132 has a total of 21 claims pending in the application; there are 4 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING DRAWINGS

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: box 216 as mentioned on **[Page 16, paragraph 0040]**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

OBJECTIONS TO THE SPECIFICATION

Specification

2. The disclosure is objected to because of the following informalities:

On **[Page 15, paragraph 0037]**, the word "*store*" in the passage "*and store store the frame 146 in the output buffer 150*" is repeated twice.

Appropriate correction is required.

Claim Objections

3. **Claims 1, 3, and 10** are objected to because of the following informalities:

Claim 1 discloses the limitation "*pacing signal*" on line 4, though earlier in the claim on line 2 the "*pace signal*" is used instead.

In **claim 3**, the phrase "*is permit*" on line 3 should instead be –*is permitted*–.

In **claim 10**, the word "*controls*" is repeated twice on line 4.

Appropriate correction is required.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim 1-10, 13, and 15-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (Patent Number US 7,369,665 B1) in view of Markre (Patent Number US 6,128,317).

As per **claim 1**, while Cheng discloses structures relating to codec **[represented by audio code 122 (FIG. 2) and DSP 811; FIG. 6A]** with outside structures handling

commands **[represented by the instruction memory 813, which is separate from data memory 815; FIG. 6A]**, Mackre discloses the idea of pacing data/commands as "*a method comprising generating a pace signal* ***(in particular the FSYNC 132 signal which defines the time interval or 'frame' during which one data word is transferred between the host processor and each CODEC (Column 3, lines 43-45), though other signals such as BCLK 130 (as noted in Column 3, lines 37-40) are involved in pacing)*** *indicative of whether sending further commands from a command buffer to a codec is permitted* ***(the contents of the output control word register are transmitted with one bit being transmitted each time the BCLK signal is asserted; Column 5, lines 48-53)****, and sending commands to the codec at a pace set by the pacing signal* ***(the rates for the BCLK and the FSYNC signals can be adjusted to accommodate a particular number and variety of CODECs required by a particular application; Column 3, lines 57-62)****.*"

Cheng and Markre are analogous art in that they are in the same field of data processing in conjunction with coders and decoders.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the system structure of data and instruction memory to CODEC/DSP of Cheng with a method of pacing data/commands as disclosed by Markre, particularly in cases where one wishes to provide for the transport of multiple variable rate data streams on a single serial link **[Column 1, lines 52-57]** in order to achieve flexibility with multiple devices **[Column 1, lines 11-14]** and to simplify overall

connections by reducing the need for multiple physical connections for multiple types of transaction protocols/timing.

As per **claim 2**, the combination of Cheng and Mackre discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Mackre further discloses "*generating the pace signal comprises periodically generating the pace signal to indicate that sending further commands to the codec is permitted* ***(the contents of the output control word register followed by the contents of each of the output data codeword registers are transmitted with one bit being transmitted each time the BCLK signal is asserted; Column 5, lines 48-53)***."

As per **claim 3**, the combination of Cheng and Mackre discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Mackre further discloses "*generating the pace signal comprises periodically generating the pace signal to indicate that sending further commands to the codec is not permit* ***(through the use of a valid bit to match the output rate of the destination CODEC relative to the FSYNC signal, data codewords flagged as 'invalid' by valid bit in control word CW are discarded; Column 5, lines 7-13)***."

As per **claim 4**, the combination of Cheng and Mackre discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Mackre discloses "*sending frames of data to the codec* ***(the system of Mackre is also capable of sending data to the CODECs 112; Column 5, lines 64-65)****, generating a new frame signal in response to each frame sent to the codec, and updating the pace signal in response to the new frame signal* ***(through the use of valid bits, the system can test whether a data codeword can***

be transmitted (Column 6, lines 45-62; Column 7, lines 1-2). The valid bit pattern is closely related to the frame rate (FSYNC); Column 7, lines 3-20)."

As per **claim 5**, the combination of Cheng and Mackre discloses "*the method*" (*see rejection to* ***claim 1*** *above*). Mackre discloses "*sending frames of data to the codec* ***(the system of Mackre is also capable of sending data to the CODECs 112; Column 5, lines 64-65)****, generating new frame signals in response to frames sent to the codec, and updating the pace signal in response to the new frame signals* ***(through the use of valid bits, the system can test whether a data codeword can be transmitted (Column 6, lines 45-62; Column 7, lines 1-2). The valid bit pattern is closely related to the frame rate (FSYNC); Column 7, lines 3-20)*** *such that the pace signal indicates that sending further commands is permitted for a first number of frames and that sending further commands is not permitted for a second number of frames* ***(through the use of a valid bit to match the output rate of the destination CODEC relative to the FSYNC signal, data codewords flagged as 'invalid' by valid bit in control word CW are discarded; Column 5, lines 7-13)***."

As per **claim 6**, the combination of Cheng and Mackre discloses "*the method*" (*see rejection to* ***claim 1*** *above*).Mackre further discloses "*receiving a pace value, and defining the second number of frames in which sending further commands is not permitted based upon the pace value* ***(through the use of a valid bit to match the output rate of the destination CODEC relative to the FSYNC signal, data codewords flagged as 'invalid' by valid bit in control word CW are discarded; Column 5, lines 7-13)***."

As per **claim 7**, while Cheng discloses the use of a DMA controller **[DSP DMA 819; FIG. 6A]**, Mackre discloses the method of data/command pacing as "*an audio controller **(the device shown can handle audio, as shown by the use of a speaker 108 and microphone 110; FIG. 1)** for a codec comprising a command pacer to control a command pace at which commands are transferred to the codec **(in particular the FSYNC 132 signal which defines the time interval or 'frame' during which one data word is transferred between the host processor and each CODEC (Column 3, lines 43-45), though other signals such as BCLK 130 (as noted in Column 3, lines 37-40) are involved in pacing)***," which also applies to "*a DMA controller to transfer commands from a command buffer of a memory to the codec based upon the command pace of the command pacer*" (with Cheng disclosing the DMA controller).

Cheng and Markre are analogous art in that they are in the same field of data processing in conjunction with coders and decoders.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the system structure of data and instruction memory to CODEC/DSP of Cheng with a method of pacing data/commands as disclosed by Markre, particularly in cases where one wishes to provide for the transport of multiple variable rate data streams on a single serial link **[Column 1, lines 52-57]** in order to achieve flexibility with multiple devices **[Column 1, lines 11-14]** and to simplify overall connections by reducing the need for multiple physical connections for multiple types of transaction protocols/timing.

As per **claim 8**, the combination of Cheng and Mackre discloses "*the audio controller*" (*see rejection to* ***claim 7*** *above*). Cheng further discloses "*the DMA controller* ***(DSP DMA 819)*** *further transfers data from the memory to the codec* ***(through the instruction memory 813 and data memory 815, with the memory 813 and 815 connected to DSP 811, the DSP DMA 819 transfers data from/to main memory; Column 8, lines 6-9; FIG. 6A)***."

As per **claim 9**, the combination of Cheng and Mackre discloses "*the audio controller*" (*see rejection to* ***claim 7*** *above*). While Markre discloses "*an output buffer to store frames* ***(the system consists of FIFO 404)****, and an audio bus interface to transfer frames from the output buffer to the codec* ***(the FIFO 404 are connected to the CODEC 122 (FIG. 4), with the CODEC 122 in turn handling audio functions such as those pertaining to speakers and microphone; FIG. 1)***," Cheng discloses "*wherein the DMA controller* ***(DSP DMA 819)*** *creates frames based upon the data and commands read from the memory* ***(the DSP DMA 819 transfers data from/to main memory; Column 8, lines 6-9)*** *and stores created frames in the output buffer for delivery to the codec* ***(the DSP DMA 819 transfers the data to the instruction memory 813 and the data memory 815; FIG. 6A)***."

As per **claim 10**, the combination of Cheng and Mackre discloses "*the audio controller*" (*see rejection to* ***claim 7*** *above*). Mackre further discloses "*the audio bus interface generates new frame signals in response to transferring frames to the codec* ***(where the system of Mackre is also capable of sending data to the CODECs 112; Column 5, lines 64-65)****, and the command pacer controls controls the command pace*

based upon the new frame signals ***(through the use of valid bits, the system can test whether a data codeword can be transmitted (Column 6, lines 45-62; Column 7, lines 1-2). The valid bit pattern is closely related to the frame rate (FSYNC); Column 7, lines 3-20)***."

As per **claim 13**, while Cheng discloses "*a system comprising memory comprising a command buffer and stream buffer* ***(the DSP DMA 819 is capable of transferring data from/to main memory to the instruction memory 813 and data memory 815; Column 8, lines 6-9; FIG. 6A)****, a codec to process data and commands* ***(the DSP 811 shown is capable of processing instruction and data from the separate memories 813 and 815)***," Markre discloses "*an audio controller* ***(the device shown can handle audio, as shown by the use of a speaker 108 and microphone 110; FIG. 1)*** *to stream data from the stream buffer to the codec* ***(the FIFO 404 are connected to the CODEC 122 (FIG. 4), with the CODEC 122 in turn handling audio functions such as those pertaining to speakers and microphone; FIG. 1)*** *and to transfer commands from the command buffer to the codec at a programmable pace* ***(the contents of the output control word register are transmitted with one bit being transmitted each time the BCLK signal is asserted (Column 5, lines 48-53), where the rates for the BCLK and the FSYNC signals can be adjusted to accommodate a particular number and variety of CODECs required by a particular application; Column 3, lines 57-62)***."

Cheng and Markre are analogous art in that they are in the same field of data processing in conjunction with coders and decoders.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the system structure of data and instruction memory to CODEC/DSP of Cheng with a method of pacing data/commands as disclosed by Markre, particularly in cases where one wishes to provide for the transport of multiple variable rate data streams on a single serial link **[Column 1, lines 52-57]** in order to achieve flexibility with multiple devices **[Column 1, lines 11-14]** and to simplify overall connections by reducing the need for multiple physical connections for multiple types of transaction protocols/timing.

As per **claim 15**, the combination of Cheng and Markre discloses "*the system*" (*see rejection to* ***claim 13*** *above*). Markre further discloses the mechanism of "*the memory further comprises a buffer descriptor list that defines the stream buffer* ***(through the use of a channel table (Column 6, lines 48-62) as well as a Transmit Finite State Machine 408 which controls the FIFO registers 404; Column 6, lines 9-12)****, and the audio controller* ***(particularly the transmit logic 114 within the clock generation module 104 that handles data transfers to the CODECs; FIGs. 1 and 4)*** *streams the data from the stream buffer per the buffer descriptor list* ***(Column 6, lines 9-12; Column 6, lines 48-66)***."

As per **claim 16**, the combination of Cheng and Markre discloses "*the system*" (*see rejection to* ***claim 13*** *above*). Mackre further discloses "*the audio controller creates frames from the data and the commands, transfers the frames to the codec, and controls the programmable pace based upon the frames transferred to the codec* ***(after the data is gathered within the register 404, it is then transmitted to the CODEC as***

represented by the lines from the registers 404 to the CODEC 122 (FIG. 4), where the contents of the output control word register (with the control word) are transmitted with one bit being transmitted each time the BCLK signal is asserted (Column 5, lines 48-53), where the rates for the BCLK and the FSYNC signals can be adjusted to accommodate a particular number and variety of CODECs required by a particular application; Column 3, lines 57-62)."

As per **claim 17**, the combination of Cheng and Markre discloses "*the system*" (*see rejection to **claim 13** above*). Mackre further discloses "*the audio controller receives a pace value, and transfers at most one command to the codec per a number of frames transferred to the codec that is equal to the pace value* ***(through the use of valid bits, the system can test whether a data codeword can be transmitted (Column 6, lines 45-62; Column 7, lines 1-2). The valid bit pattern is closely related to the frame rate (FSYNC); Column 7, lines 3-20)***."

As per **claim 18**, while Cheng discloses structures relating to codec **[represented by audio code 122 (FIG. 2) and DSP 811; FIG. 6A]** with outside structures handling commands **[represented by the instruction memory 813, which is separate from data memory 815; FIG. 6A]**, which applies to the limitation "*a machine-readable medium comprising a plurality of instructions*," Mackre discloses the idea of pacing data/commands as "*in response to being executed, result in a computing device storing commands in a command buffer of a memory, setting a command pace, and transferring the commands to a codec at the command pace* ***(the contents of the output control word register (with the control word) are transmitted with one bit***

being transmitted each time the BCLK signal is asserted (Column 5, lines 48-53), where the rates for the BCLK and the FSYNC signals can be adjusted to accommodate a particular number and variety of CODECs required by a particular application; Column 3, lines 57-62)."

Cheng and Markre are analogous art in that they are in the same field of data processing in conjunction with coders and decoders.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the system structure of data and instruction memory to CODEC/DSP of Cheng with a method of pacing data/commands as disclosed by Markre, particularly in cases where one wishes to provide for the transport of multiple variable rate data streams on a single serial link **[Column 1, lines 52-57]** in order to achieve flexibility with multiple devices **[Column 1, lines 11-14]** and to simplify overall connections by reducing the need for multiple physical connections for multiple types of transaction protocols/timing.

As per **claim 19**, the combination of Cheng and Markre discloses "*the machine-readable medium*" (*see rejection to **claim 18** above*). Mackre further discloses "*the plurality of instructions further result in the computing device storing data in a stream buffer of the memory **(assertion of the Frame Synce (FSYNC) signal starts the accumulation where a single bit is serially shifted into a codeword length register every time the Byte Clock (BCLK) 130 signal is asserted; Column 6, lines 1-4)**, and transferring the data from the stream buffer to the codec in frames **(after the data is***

gathered within the register 404, it is then transmitted to the CODEC as represented by the lines from the registers 404 to the CODEC 122; FIG. 4)."

As per **claim 20**, the combination of Cheng and Markre discloses "*the machine-readable medium*" (*see rejection to* ***claim 18*** *above*). Mackre further discloses "*the plurality of instructions further result in the computing device placing the commands in a portion of the frames transferred to the codec that is based upon the command pace* ***(through the use of valid bits, the system can test whether a data codeword can be transmitted (Column 6, lines 45-62; Column 7, lines 1-2). The valid bit pattern is closely related to the frame rate (FSYNC); Column 7, lines 3-20)***."

As per **claim 21**, the combination of Cheng and Markre discloses "*the machine-readable medium*" (*see rejection to* ***claim 18*** *above*). Mackre further discloses "*the plurality of instructions further result in the computing device processing responses of the codec from a response buffer of the memory* ***(the data bits received from each CODEC are clocked into a corresponding register 310 (Column 5, lines 28-33) within a Receive Logic 116 portion of the MFCD 104 (FIG. 3), with the data then transmitted to the host processor; FIG. 1)***."

6. **Claims 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (Patent Number US 7,369,665 B1) and Markre (Patent Number US 6,128,317) in view of "The High-Level Entity Management System" by Craig Partridge and Glenn Trewitt (henceforth known as Partridge et al.).

As per **claim 11**, the combination of Cheng and Markre discloses "*the audio controller*" (*see rejection to* ***claim 7*** *above*). Though Markre discloses the idea of pacing

data/commands as disclosed in the limitation "*and a pace signal generator to generate a pace signal…that is indicative of the command pace* ***(the rates for the BCLK and the FSYNC signals can be adjusted to accommodate a particular number and variety of CODECs required by a particular application; Column 3, lines 57-62)***," the combination of Cheng and Markre does not disclose the use of a roll-over counter as disclosed in the limitation "*the command pacer comprises a roll-over counter to update a count in response to each frame transferred to the codec, and a pace signal generator to generate a pace signal based upon the count of the roll-over counter that is indicative of the command pace*," which Partridge et al. discloses **[Page 40, paragraph 3 under section entitled "Low Level Data Types"]**.

Cheng, Markre, and Patridge et al. are analogous art in that they are in the same field of data processing and device interfacing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the audio controller as disclosed by the combination of Cheng and Markre with a roll-over counter as disclosed by Partridge et al., which notes the disadvantages of using other types of counters (such as the latch counter that must be reset, yet it is difficult to determine under what circumstances such a counter *should* be reset), while the advantages of a roll-over counter include readable, little or no required maintenance, and if the counters are large enough will roll-over only infrequently **[Page 40, paragraph 3 under section entitled "Low Level Data Types"]**.

As per **claim 12**, the combination of Cheng, Markre, and Partridge et al. discloses "*the audio controller*" (*see rejection to* ***claim 11*** *above*). While Markre

discloses the idea of pacing data/commands as **[the rates for the BCLK and the FSYNC signals can be adjusted to accommodate a particular number and variety of CODECs required by a particular application; Column 3, lines 57-62]**, Partridge et al. further discloses the idea, as it relates to a roll-over counter, of "*the pace signal generator generates the pace signal to allow further commands to the codec when the count of the roll-over counter has a predetermined relationship to a predetermined count of the roll-over counter* ***(counts of various functions performed are an important management tool, such as in instances where an abstraction that incorporated the notion that a count had reached a limit is needed (Page 40, paragraph 3 under section entitled "Low Level Data Types"), which is interpreted as an action is taken when a particular counter value (which applies to a 'predetermined count') is achieved)***."

7. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng (Patent Number US 7,369,665 B1) and Markre (Patent Number US 6,128,317) in view of Winkler et al. (Publication Umber US 2004/0024948 A1).

As per **claim 14**, the combination of Cheng and Markre discloses "*the system*" (*see rejection to* ***claim 13*** *above*). However, the combination of Cheng and Markre does not explicitly disclose the use of a response buffer as disclosed in the limitation "*the memory further comprises a response buffer, the codec further generates responses in response to processing the commands, and the audio controller further streams the responses from the codec to the response buffer.*"

Winkler et al. discloses the use of a response buffer as "*the memory further comprises a response buffer* ***(represented by buffer 510)****, the codec further generates responses in response to processing the commands* ***(each response in buffer 510 is associated with a command tag (e.g. TAG1-3), which are data items used to uniquely identify upstream commands; FIG. 5; Page 3, paragraph 0037)****, and the audio controller further streams the responses from the codec to the response buffer* ***(the response buffer 510 stores the response data in the form the data was received by the receive engine from the HyperTransport interface unit; Page 3, paragraph 0039)***."

Cheng, Markre, and Winkler et al. are analogous art in that they are in the same field of data processing and device interfacing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the audio controller as disclosed by the combination of Cheng and Markre with a response buffers as disclosed by Winkler et al., which is important in cases where there exists outstanding read requests (such as commands where the corresponding data/response is not instantaneous), which in turn require in such cases to buffer responses **[Page 2, paragraph 0014]**.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

8. As required by **M.P.E.P. 609(c)**, the applicant's submission of the Information Disclosure Statement dated November 25, 2003, is acknowledged by the examiner and the cited references have been considered in the examination of the claims now

pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

RELEVENT ART CITED BY THE EXAMINER

9. The following prior art made of record and relied upon is citied to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c).**

10. The following references teach the memory/device access, particularly for parallel components:

U.S. PATENT NUMBERS:

2003/0204276 A1

2003/0001878 A1

5,297,231

5,812,875

6,323,867 B1

6,434,633 B1

NON-PATENT LITERATURE:

Greg Partridge and Glenn Trewitt. "The High-Level Entity Management System (HEMS)." *IEEE Network*. March 1988: 37-42.

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

11. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P 707.07(i):**

a(1). CLAIMS REJECTED IN THE APPLICATION

12. Per the instant office action, claims 1-21 have received a first action on the merits and are subject of a first action non-final.

13. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HENRY YU whose telephone number is (571)272-9779. The examiner can normally be reached on Monday to Friday, 8:00 AM to 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TARIQ HAFIZ can be reached on (571) 272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/H. Y./
Examiner, Art Unit 2182
September 30, 2008

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182